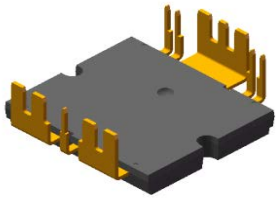
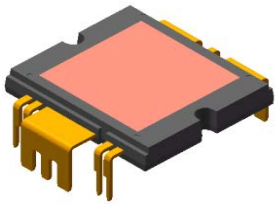
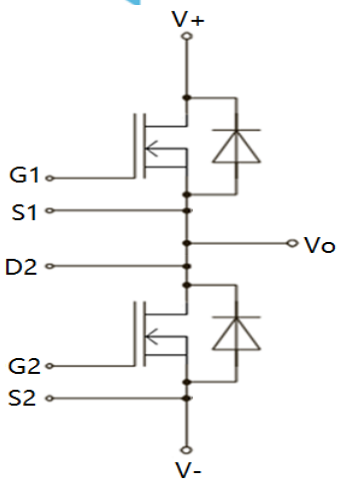
SLC500MM10SCT2







1 Description

Features:

- Low Rdson to Minimize Conductive Loss
- Halfbridge, Easy paralleling
- High Ruggedness
- N-channel power MOSFET module

Application:

- AC Motor control
- Power supply

Table 1: Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(ON)typ.}$	1.05	mΩ
I_D	500	A
Q_{OSS}	188	nC
Q_G	258	nC

RoHS

Type / Ordering Code	Package	Marking	Related Links
SLC500MM10SCT2	T2		

Revision: 2021-08-26, Rev1.4

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
V1.1	2020-12-12	Parameter correction
V1.2	2021-01-20	Updated the parameter of Rthjc
V1.3	2021-08-05	Chart revision
V1.4	2021-09-13	Parameter correction

2 Maximum ratings

at T_j = 25 ℃, unless otherwise specified

Table 2 Maximum Ratings (PER ARM)

Parameter	symbol	Value			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain-source voltage	V_{DS}	100	–	–	V	V_{GS}=0, I_D=250uA, T_j=25℃
Continuous drain current	I_D	–	500	–	A	V_{GS}=10V, T_C=25℃, R_{thJC}=0.18℃/W
		–	360	–		V_{GS}=10V, T_C=100℃, R_{thJC}=0.18℃/W
Pulsed drain current	$I_{D,pulse}$	–	1200	–	A	T_C=25℃
Avalanche energy, single pulse	E_{AS}	–	1024	–	mJ	L=2mH, R_g=25 Ω
Gate-Source voltage	V_{GS}	-20	–	20	V	-
Power dissipation	P_{tot}	–	694	–	W	T_C=25℃
Operating & storage temperature	T_j, T_{stg}	-55	–	150	℃	-

3 Thermal characteristics

Table 3 Thermal characteristics (PER ARM)

Parameter	symbol	Value			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	–	0.18	–	K/W	Junction to heat dissipation copper plate

4 Electrical characteristics

Table 4 Static Characteristic

Parameter	symbol	Value			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain-source breakdowm voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0, I_D=250uA, T_j=25℃
Gate threshold voltage	$V_{GS(th)}$	2.0	2.7	4.0	V	V_{DS}=V_{GS}, I_D=250uA, T_j=25℃
Zero gate voltage drain current	I_{DSS}	-	-	5.0	uA	V_{DS}=100V, V_{GS}=0, T_j=25℃
		-	-			V_{DS}=100V, V_{GS}=0, T_j=125℃
Gate-source leakage current	I_{GSS}	-	50	400.0	nA	V_{DS}=0V, V_{GS}=20V, T_j=25℃
Drain-source on-state resistance	$R_{DS(ON)}$	-	1.2	1.7	mΩ	V_{GS}=6V, I_D=75A, T_j=25℃
		-	1.05	1.6		V_{GS}=10V, I_D=100A, T_j=25℃
Gate resistance	R_G	-	1	-	Ω	V_{GS}=0, V_{DS}=0, f=1MHz
Transconductance	g_{fs}	-	460	-	S	V_{DS}=40V, I_D=200A

Table 5 Dynamic characteristics

Parameter	symbol	Value			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input Capacitance	C_{iss}	-	29.8	-	nF	V_{GS}=0 V_{DS}=40V f=1.0MHz
Output capacitance	C_{oss}	-	4.7	-	nF	
Reverse transfer capacitance	C_{rss}	-	1.7	-	pF	
Turn-on delay time	$t_{d(on)}$	-	240.0	-	ns	V_{DD}=72V V_{GS}=15V I_D=290A $R_{G,ext}$=5.1Ω
Rise time	t_r	-	240	-	ns	
Turn-off delay time	$t_{d(off)}$	-	600	-	ns	
Fall time	t_f	-	200	-	ns	

Table 6 Gate charge characteristics

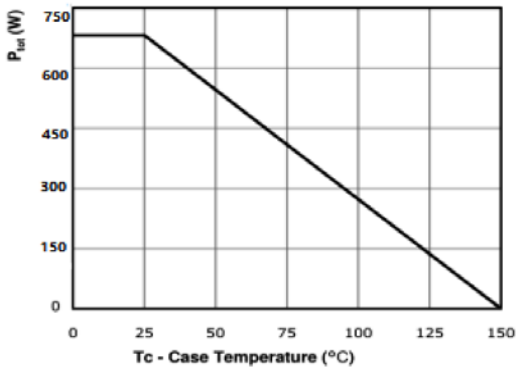
Parameter	symbol	Value			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	–	100	–	nC	V_{DD}=40V, I_D=100A, V_{GS}=10V
Gate charge at threshold	$Q_{g(th)}$	–	41.0	–	nC	V_{DD}=40V, I_D=100A, V_{GS}=10V
Gate to drain charge	Q_{gd}	–	92	–	nC	V_{DD}=40V, I_D=100A, V_{GS}=10V
Gate charge total	Q_g	–	258	–	nC	V_{DD}=40V, I_D=100A, V_{GS}=10V
Gate plateau voltage	$V_{plateau}$	–	5	–	V	V_{DD}=40V, I_D=100A, V_{GS}=10V
Output charge	Q_{oss}	–	188	–	nC	V_{DD}=40V, V_{GS}=0V

Table 7 Reverse diode

Parameter	symbol	Value			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	–	500	–	A	T_j=25℃
Diode pulse current	$I_{S,pulse}$	–	1200.0	–	A	T_j=25℃
Diode forward voltage	V_{SD}	–	0.78	1.2	V	V_{GS}=0, I_S=150A, T_j=25℃
Reverse recovery time	t_{rr}	–	33	–	ns	V_R=50V I_F=50A di/dt=200A/us
Reverse recovery charge	Q_{rr}	–	58	–	nC	

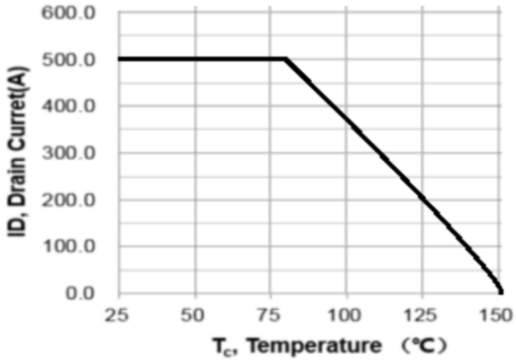
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



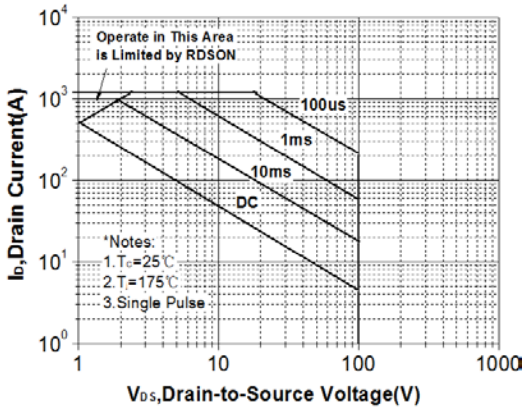
$P_{tot}=f(T_C)$

Diagram 2: Drain current



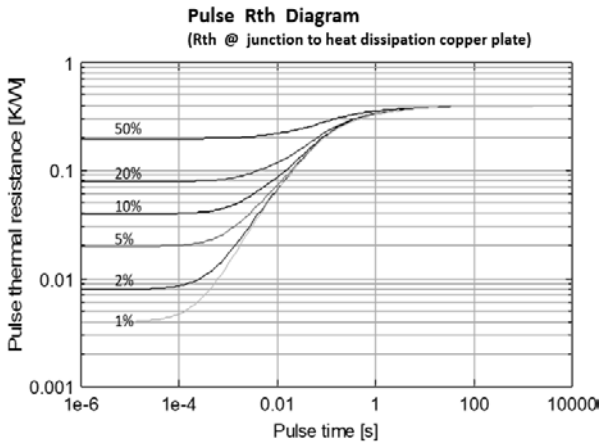
$I_D=f(T_C)$

Diagram 3: Safe operating area



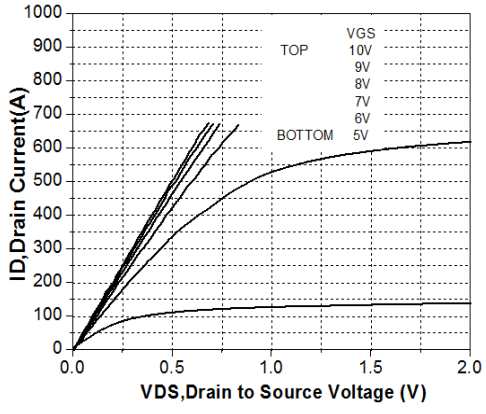
$I_D=f(V_{DS})$

Diagram 4: Pulse thermal resistance



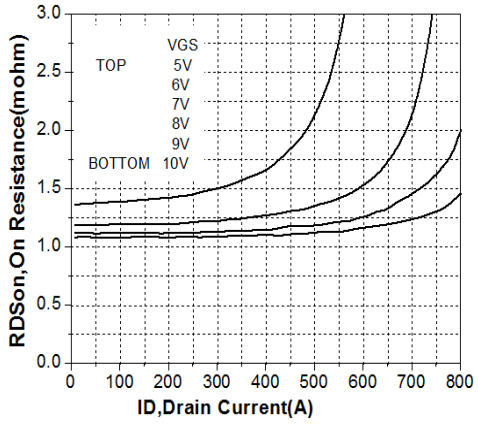
Pulse $R_{th}=f(T*D)$; D=Duty cycle; T=cycle

Diagram 5: Typ. output characteristics



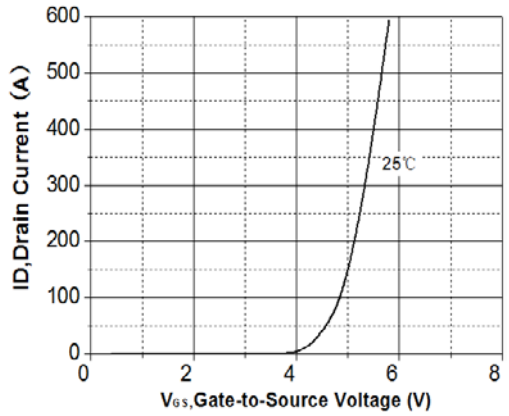
$I_D=f(V_{DS})$; T_j=25℃; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



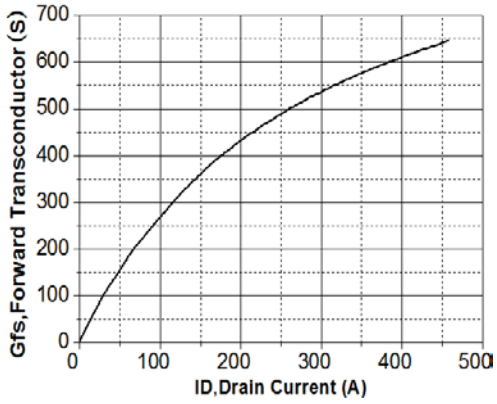
$R_{DS(on)}=f(I_D)$; T_j=25℃; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



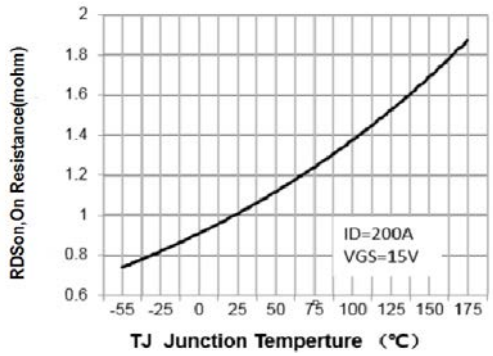
$I_D=f(V_{GS})$;Tj=25℃

Diagram 8: Typ. forward transconductance



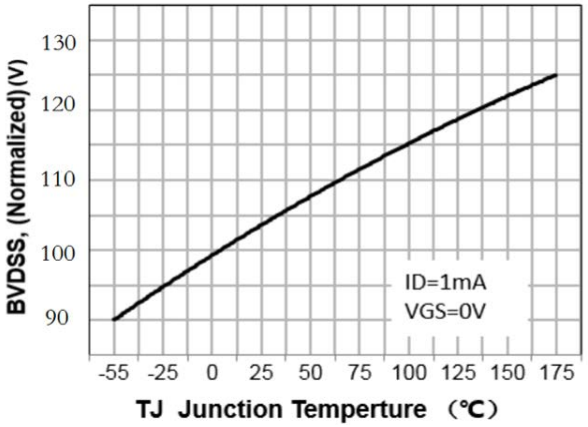
$g_{fs}=f(I_D)$;T_j=25℃

Diagram 9: Drain-source on-state resistance



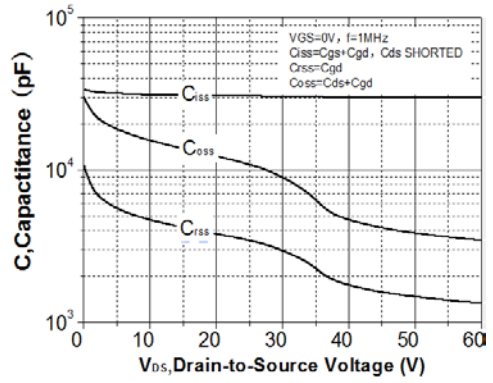
$R_{DS(on)}=f(T_j)$;I_D=200A;V_{GS}=15V

Diagram 10: Drain-source breakdown voltage



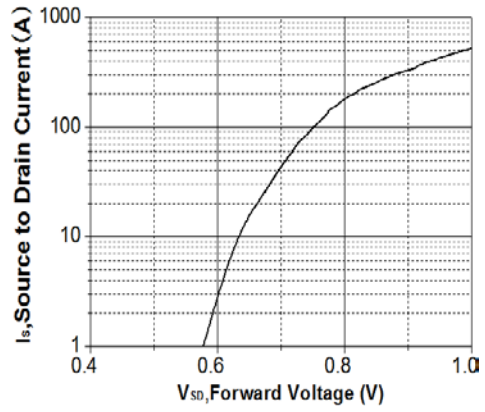
$V_{BR(DSS)}=f(T_j)$;I_D=1mA;VGS=0V

Diagram 11: Typ. Capacitances



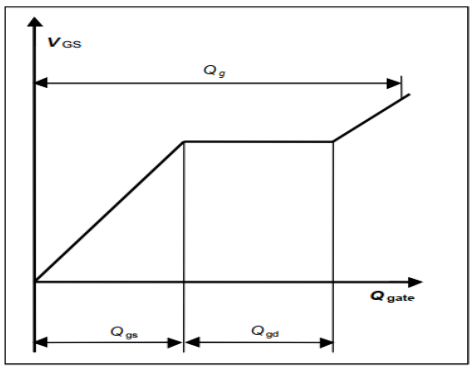
C=f(V_{DS});V_{GS}=0V;f=1MHz

Diagram 12: Forward characteristics of reverse diode



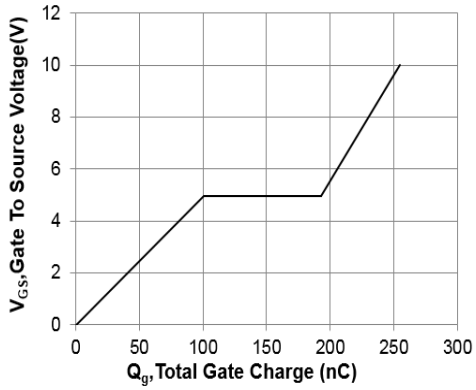
$I_S=f(V_{SD})$

Diagram 13:Gate charge waveforms



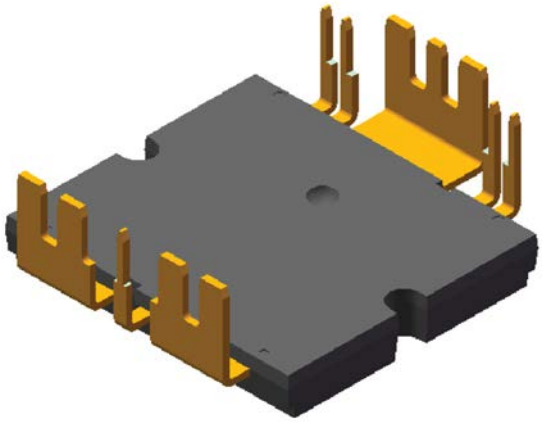
Gate charge waveforms

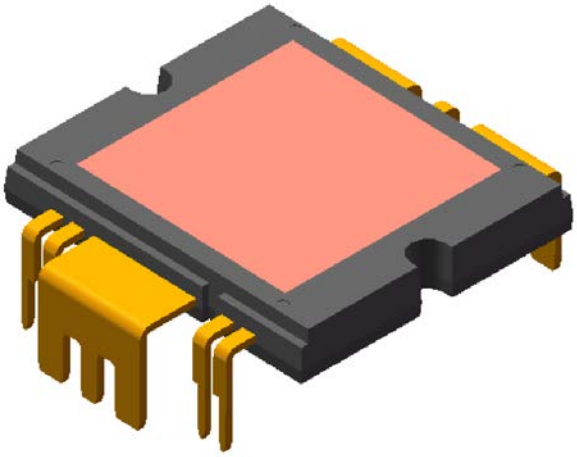
Diagram 14: Typ. gate charge

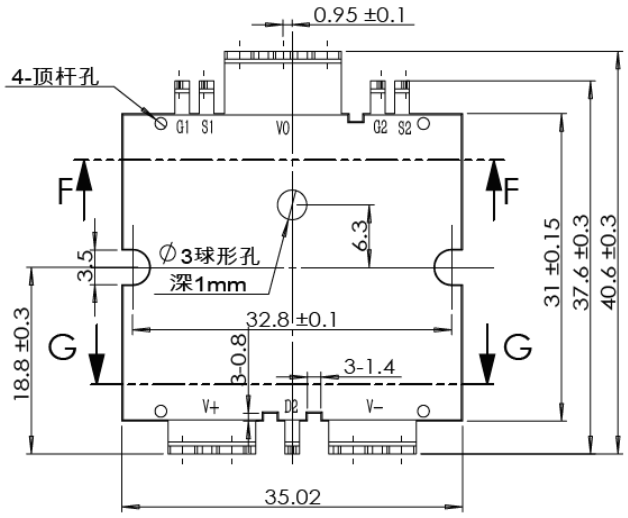


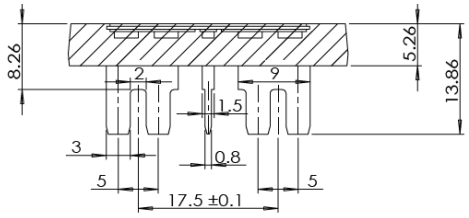
$V_{GS}=f_{(Qgate)}$;I_D=100A

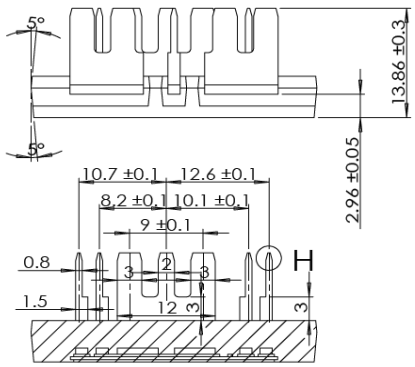
6 Package Outlines

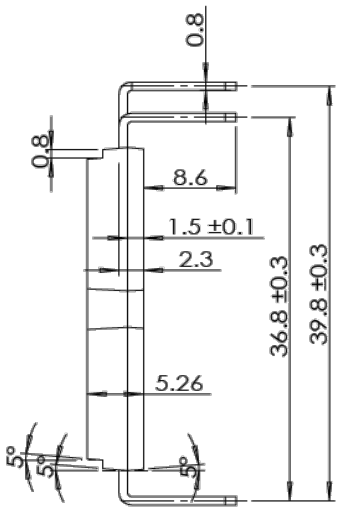


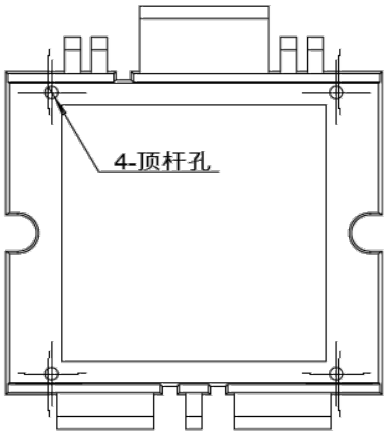


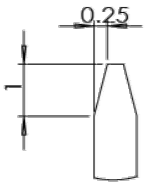












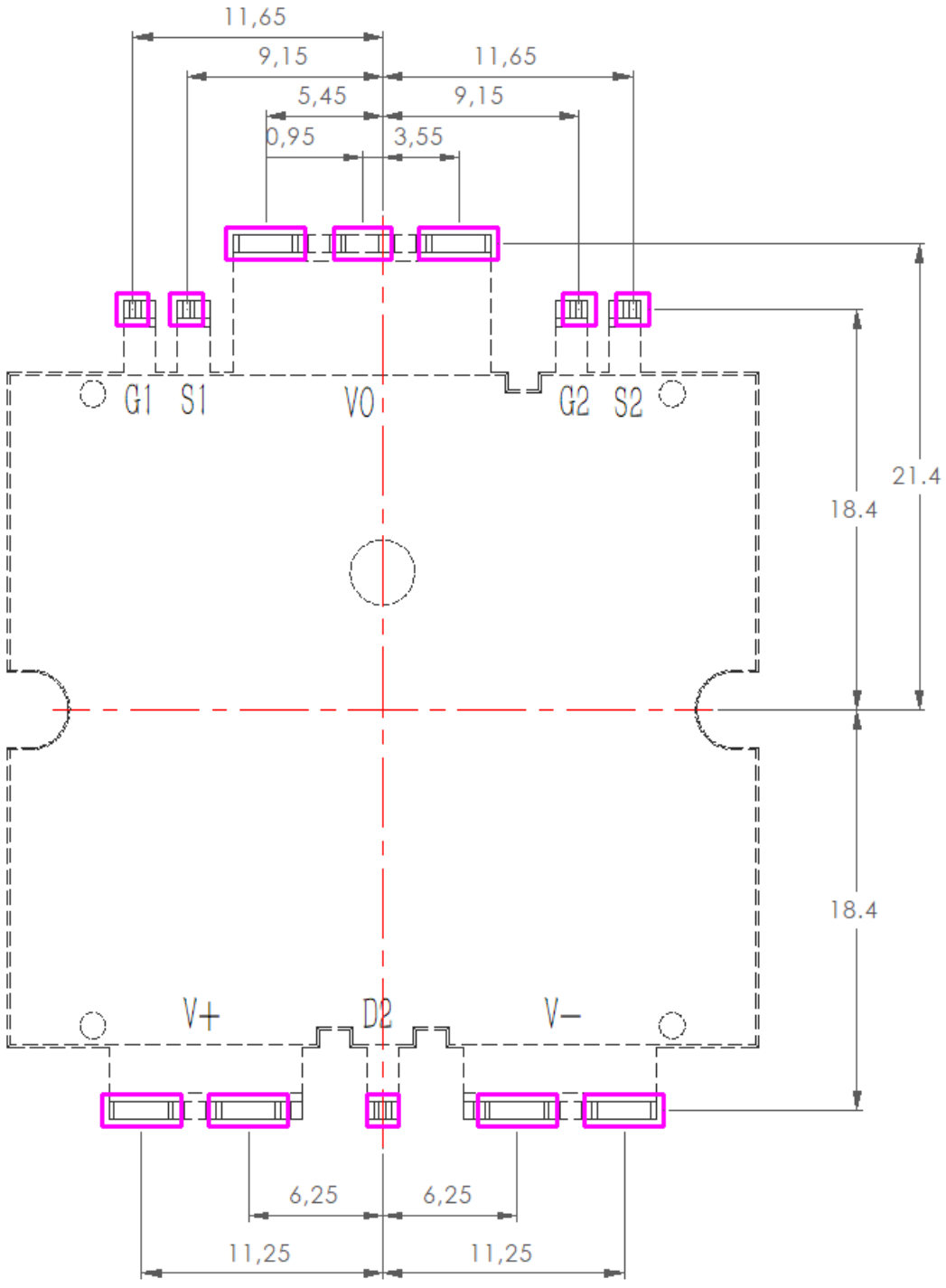
局部视图 H

比例 10 : 1

建议安装方式：

1、压片安装。

Suggested pad layout



注：所有公差±0.3mm